WHAT IS CLAIMED IS:

1. A flash EEPROM unit cell comprising:

a substrate on which field oxide layers are formed for isolating unit cells;

a floating gate dielectric layer formed between the adjacent field oxide layers, wherein the floating gate dielectric layer includes a first dielectric layer and a second dielectric layer which are connected in parallel between a source and a drain formed on the substrate, and the thickness of the first dielectric layer is thicker than the second dielectric layer;

a floating gate formed on the floating gate dielectric layer;

a control gate dielectric layer formed on the floating gate; and

a control gate formed on the control gate dielectric layer.

2. The flash EEPROM unit cell of claim 1, wherein the second dielectric layer works as a tunnel oxide layer for inducing an electron-injection into the floating gate and an electron-emission from the floating gate.

3. The flash EEPROM unit cell of claim 1, wherein the surface area of the first dielectric layer is substantially equal to that of the second dielectric layer.

4. The flash EEPROM unit cell of claim 1, wherein the thickness of the first dielectric layer is substantially equal to that of a dielectric layer of a peripheral devices formed in a flash EEPROM device to control the flash EEPROM device.

5. The flash EEPROM unit cell of claim 1, wherein the floating gate is formed only on the floating gate dielectric layer.

6. A flash EEPROM array architecture comprising:

a plurality of bit lines;

a plurality of word lines which intersect the plurality of bit lines; and

a memory string including a plurality of unit cells serially connected to one of the bit lines,

wherein each of the unit cells is connected to a respective word line, and the unit cell includes a first sub-cell and a second sub-cell connected in parallel between a source and a drain, and a capacitance of a dielectric layer under a floating gate of the first sub-cell is smaller than that of dielectric layer under a floating gate of the second sub-cell.

7. The flash EEPROM array architecture of claim 6, wherein the dielectric layer of the first sub-cell is thicker than that of the dielectric layer of the second sub-cell.

8. The flash EEPROM array architecture of claim 6, wherein a control gate of the first sub-cell and a control gate of the second sub-cell are connected to the same word line, and the floating gate of the first sub-cell is connected to the floating gate of the second sub-cell.

9. The flash EEPROM array architecture of claim 6, wherein the floating gate of the first sub-cell and the floating gate of the second sub-cell are connected together, and the control gate of the first sub-cell and the control gate of the second sub-cell are connected together.

10. The flash EEPROM array architecture of claim 6, wherein the floating gate of the first sub-cell and the floating gate of the second sub-cell are formed between field oxide layers for separating the unit cells.

11. A flash EEPROM array architecture comprising:

a plurality of bit lines;

a plurality of word lines which intersect the plurality of bit lines; and

a plurality of unit cells formed at the intersection of the bit lines and the word lines;

wherein the unit cells at a row are connected to a word line; each of the unit cells includes a first sub-cell and a second sub-cell connected in parallel between a source and a drain; the sources of the unit cells are connected to a common source line; the drains of the unit cells at a column is connected to a bit line; and a capacitance of dielectric layer under a floating gate of the first sub-cell is smaller than that of dielectric layer under a floating gate of the second sub-cell.

12. The flash EEPROM array architecture of claim 11, wherein the dielectric layer of the first sub-cell is thicker than that of the dielectric layer of the second sub-cell.

13. The flash EEPROM array architecture of claim 11, wherein a control gate of the first sub-cell and a control gate of the second sub-cell are connected to the same word line, and the floating gate of the first sub-cell is connected to the floating gate of the second sub-cell.

14. The flash EEPROM array architecture of claim 11, wherein the floating gate of the first sub-cell and the floating gate of the second sub-cell are connected together and the control gate of the first sub-cell and the control gate of the second sub-cell are connected together.

15. The flash EEPROM array architecture of claim 11, wherein the floating gate of the first sub-cell and the floating gate of the second sub-cell are formed between adjacent field oxide layers for separating the unit cells.